

## PATENT ABSTRACTS OF JAPAN

(11)Publication number : 11-074487

(43)Date of publication of application : 16.03.1999

(51)Int.Cl.

H01L 27/108  
H01L 21/8242  
H01L 21/28  
H01L 21/768

(21)Application number : 10-179870

(71)Applicant : FUJITSU LTD

(22)Date of filing : 26.06.1998

(72)Inventor : YAMAUCHI HIDEAKI

(30)Priority

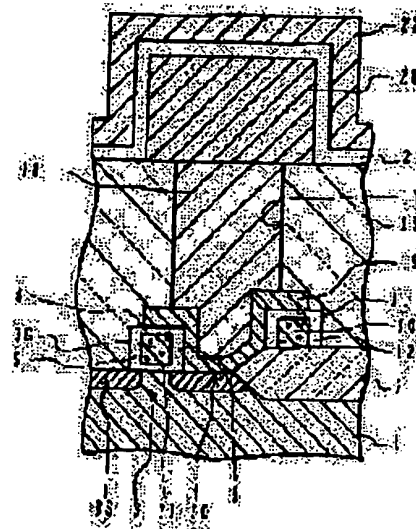
Priority number : 09175051 Priority date : 30.06.1997 Priority country : JP

## (54) SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

(57)Abstract:

**PROBLEM TO BE SOLVED:** To prevent inter-migration of the compositions of a semiconductor region and a conductive member by a method wherein the semiconductor region out of an insulating region and the semiconductor region, which are exposed on a substrate, is covered with a barrier layer, this barrier layer is covered with an interlayer insulating film, through which a contact hole penetrates, and the conductive member is buried in this hole.

**SOLUTION:** A MOS transistor 3 is formed on an active region exposed on a silicon substrate 1. A drain region 3D is covered with a barrier layer 15 and an interlayer insulating film 16 is formed on the surface of the substrate in such a way as to cover the layer 15. A contact hole 17 is formed in this film 16 on the upper surface on the inner side of the layer 15 and a conductive member 18 is buried in the interior of this hole 17. A charge storage electrode 20 is formed on the upper surface of the member 18 and moreover, a capacitor insulating film 21 is formed on the film 16. The layer 15 prevents inter-migration of the capacitors compositions of the substrate 1 and the member 18 and a solid phase reaction due to the compositions to raise the connection between the silicon substrate and a metal film and at the same time, the layer 15 is prevented from being oxidized at the time of a treatment of the layer 15.



## LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]